AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

Claims 1-19: (Cancelled).

Claim 20 (Currently Amended): An unpredictable microprocessor or microcomputer comprising:

~~-a processor;~~

-a main memory including an operating system, a main program, and a secondary program, wherein said secondary program is not related to the main program;

-a first working memory;

- a second working memory;

- a processor for executing instructions from said main memory, first working memory or second working memory;

- a bus connecting the processor to the main memory, the first working memory and the second working memory;

~~-a~~ switching means for making said processor unpredictable, said switching means switching, at a random interrupt, while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories, said switching means comprising:

- access registers associated with each memory; ~~including~~

- at least one first block of registers for storing the operating context of the programs in the main memory; and;

-a switching circuit for enabling one of the working memories and controlling the access registers associated with each memory ~~and controlled by said switching circuit~~.

Claim 21 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 20, further ~~including~~ comprising a second block of registers for storing the operating context of the secondary program.

Claim 22 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, further including means for de-correlating the running of the programs from an isochronous clock.

Claim 23 (Currently Amended): The microprocessor or microcomputer according to claim ~~20~~21, characterized in that the main program can enable or inhibit the switching means ~~mechanism or mechanisms~~ by loading the switching circuit for switching and enabling the working memories and the first block and second block ~~blocks~~ of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program.

Claim 24 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the second working memory and its access registers are substituted for the first working memory and its access registers in utilization by the main program.

Claim 25 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 22, characterized in that the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, ~~a~~ the random interrupt

for desynchronizing the running of the programs in the processor, by randomly jumping to the secondary program.

Claim 26 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 23, further including means for de-correlating the running of the programs from an isochronous clock, characterized in that the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program.

Claim 27 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 23, further including means for de-correlating the running of the programs from an isochronous clock, characterized in that the switching means ~~for switching working memories~~ is controlled by the processor and its program, by the ~~random interrupt system~~ de-correlating means, by a timer, or by any combination of at least two of the three named elements.

Claim 28 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the switching means ~~for switching working memories~~ is enabled by being loaded by the processor running a sequence in the main program ~~sequence~~.

Claim 29 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program uses a working space identical to that of the main program in the main memory.

Claim 30 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program uses a working space smaller than that of the main program.

Claim 31 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the switching means carry out the substitution of the memories and the associated contexts within the execution cycle of an instruction from the microprocessor.

Claim 32 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the secondary program does not modify the general operating context of the main program in order to allow the main program to return without having to reestablish said context.

Claim 33 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 32, characterized in that the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program.

Claim 34 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that it further comprises means for substituting the memory of the secondary program for the memory of the main program.

Claim 35 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the main program can use the first working memory and~~/or~~ the second working memory alternately or simultaneously.

Claim 36 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 23, characterized in that loading of the switching circuit makes it possible to mask or unmask de-correlating interrupts.

Claim 37 (Previously Presented): The unpredictable microprocessor or microcomputer, according to claim 25, characterized in that an interrupt triggered by the secondary program effects return to the main program after the switching register has been properly loaded, by executing an instruction of the main program or the secondary program, in order to unmask the interrupts.

Claim 38 (Previously Presented): The unpredictable microprocessor or microcomputer, according to claim 20, characterized in that the microprocessor or microcomputer is embodied in a monolithic integrated circuit.

Claim 39 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 21, further including means of de-correlating the run-through of the programs with respect to an isochronal clock.

Claim 40 (Cancelled)

Claim 41 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 21 characterized in that the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory.

Claim 42 (Previously Presented): The unpredictable microprocessor or microcomputer according to claim 22 characterized in that the de-correlating means comprise a random generator.

Claims 43 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 25 characterized in that the ~~means of~~ de-correlation means include a time counting system independent of the processor for enabling, at the end of a time count, ~~the triggering of~~ an interruption trigger to return from the secondary program to the main program.

Claim 44 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 25 characterized in that the switching means ~~of switching the working memories~~ is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or a combination of at least two out of the three named elements.

Claim 45 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 22 characterized in that the main program is adapted to enable or inhibit the switching ~~mechanism or mechanisms~~ means by loading the switching circuit

of working memories and of the memorization register blocks associated with each respective working memory.

Claim 46 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 22 characterized in that the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by ~~a~~ the main program, with said first working memory and the associated access registers of the first working memory.

Claim 47 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 26 characterized in that the switching means ~~of switching the working memories~~ is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or by a combination of at least two out of the three named elements.

Claim 48 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 25 characterized in that the ~~interruption~~ interrupt circuit triggers the random number generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program.

Claim 49 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 26 characterized in that the de-correlation means include ~~includes~~ a time counting system independent of the processor for enabling, at the end of a time count, the triggering of ~~an interruption~~ the random interrupt to return from the

secondary program to the main program, and the switching means ~~of switching the working memories~~ is controlled by one of the microprocessors and the program thereof, the random interruption system, a time counter or by a combination of at least two of the three named elements.

Claim 50 (Currently Amended): The unpredictable microprocessor or microcomputer according to claim 21 characterized in that the switching means ~~of switching the working memories~~ is confirmed by loading from the processor executing a main program sequence.